IN THE CLAIMS:

Please amend claims 1, 7-13, 20-23 and 25 as indicated in the following.

Claims Listing:

1. (Currently Amended) Image processing circuitry, comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image ~~pipeline~~pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

2. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said two-dimensional mode and to perform texture mapping in said three-dimensional mode.

3. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said two-dimensional mode and to blend samples from a plurality of texture maps in said three-dimensional mode.

4. (Previously Presented) The image processing circuitry set forth in Claim 2 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said two-dimensional mode and to perform alpha blending in said three-dimensional mode.

5. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein the image processing circuitry is operable to support at least one MPEG standard.

6. (Original) The image processing circuitry set forth in Claim 1 further comprising an alpha blend sub-circuitry that is operable to process at least 8- and 9-bit signed values.

7. (Currently Amended) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising ~~the steps of~~:

determining whether said dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode;

performing motion compensation operations associated with said two- dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and

performing rasterization operations associated said three-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode.

8. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising ~~the steps of~~:

sampling a plurality of reference frames in said two-dimensional mode; and

performing texture mapping in said three-dimensional mode.

9. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising ~~the step of~~ blending one of samples from a plurality of reference frames in said two-dimensional mode and samples from a plurality of texture maps in said three-dimensional mode.

10. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 8 further comprising ~~the steps of~~:

processing said plurality of reference frames using error terms in said two-dimensional mode; and

performing alpha blending in said three-dimensional mode.

11. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising ~~the step of~~ switching from said three-dimensional mode to said two-dimensional mode to perform motion compensation in accordance with at least one MPEG standard.

12. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 10 wherein [[said]]performing alpha blending [[step]]further comprises ~~the step of~~ processing at least 8- and 9-bit signed values.

13. (Currently Amended) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising ~~the step of~~ controlling said dual mode sub-processing circuitry.

14. (Previously Presented) Mode control circuitry for use in an image processing system having a two-dimensional image pipeline having a plurality of stages including a first stage and a last

stage that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising:

dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and

a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode.

15. (Previously Presented) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to sample a plurality of reference frames in said two-dimensional mode and to perform texture mapping in said three-dimensional mode.

16. (Previously Presented) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said two-dimensional mode and to blend samples from a plurality of texture maps in said three-dimensional mode.

17. (Previously Presented) The mode control circuitry set forth in Claim 15 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said two-dimensional mode and to perform alpha blending in said three-dimensional mode.

18. (Original) The mode control circuitry set forth in Claim 14 wherein said dual

mode sub-processing circuitry is operable to support at least one MPEG standard.

19. (Original) The mode control circuitry set forth in Claim 14 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

20. (Currently Amended) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising ~~the steps of~~:

determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and

controlling said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode.

21. (Currently Amended) The method of operating said mode control circuitry set forth in Claim 20 further comprising ~~the steps of~~:

sampling a plurality of reference frames in said two-dimensional mode; and

performing texture mapping in said three-dimensional mode.

22. (Currently Amended) The method of said operating mode control circuitry set forth in Claim 20 further comprising ~~the steps of~~:

blending samples from a plurality of reference frames in said one two-dimensional mode; and

blending samples from a plurality of texture maps in said other three-dimensional mode.

23. (Currently Amended) The method of operating said mode control circuitry set forth in Claim 21 further comprising ~~the steps of~~:

processing said plurality of reference frames using error terms in said one two-dimensional mode; and

performing alpha blending in said three-dimensional mode.

24. (Previously Presented) The method of operating said mode control circuitry set forth in Claim 20 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

25. (Currently Amended) The method of operating mode control circuitry set forth in Claim 20 further comprising ~~the step of~~ controlling said dual-mode sub-processing circuitry using an alpha blend sub-circuitry that is operable to process at least 8-bit and 9- bit signed values.

26. (Previously Presented) A media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in

said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

27. (Previously Presented) Processing apparatus comprising:

a first specialty pipeline having a plurality of stages including a first stage and a last stage;

a second specialty pipeline having a plurality of stages including a first stage and a last stage; and

dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of said first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of said second specialty pipeline.

28. (Previously Presented) The processing apparatus of claim 27 wherein said first specialty pipeline comprises a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of a display system.

29. (Previously Presented) The processing apparatus of claim 28 wherein said second specialty pipeline is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system.

30. (Previously Presented) The processing apparatus of claim 29 wherein when in said first mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline and when in said second mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline.